BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

Post-Graduate
ECE-606
CAD of Electronics

PART #2

Lecture #1
CAD Fundamentals

Instructor:
Dr. Ahmad El-Banna

DECEMBER 2014

Agenda

- Course Objectives (Part#2)
- Course Information
- Trend in microelectronics
- The design challenges
- Different design paradigms
- The test problems

Course Objectives PART #2

- ***Learn the basic concepts of CAD Design for electronics.***
- ***Electronic system design at high levels of abstraction.***
- ***Design, implement, test and validate the electronics systems.***

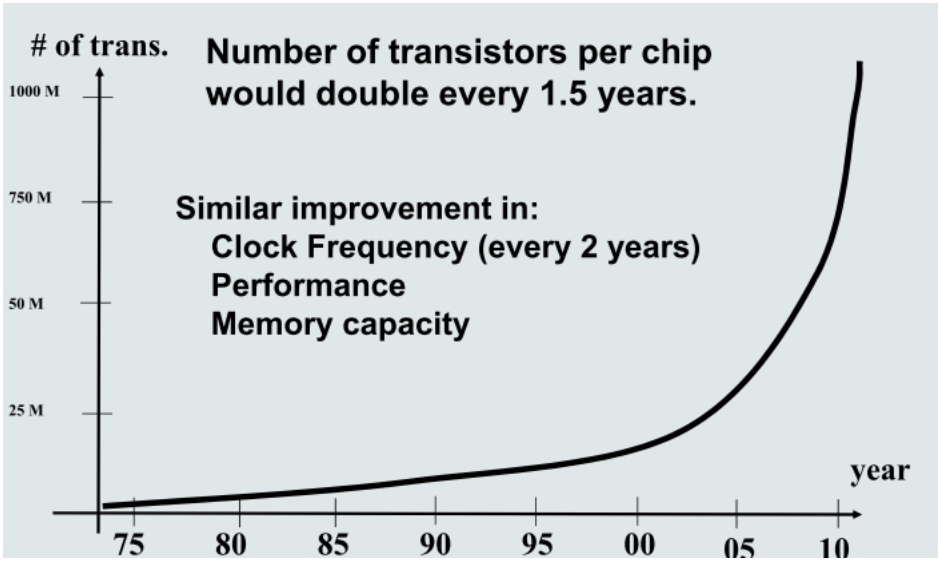
- *Study the basics of VHDL language and its use in the design/synthesis process.*
- *Perform Simulations using simulation tools.*
- *Implement digital circuits design on FPGA platform.*

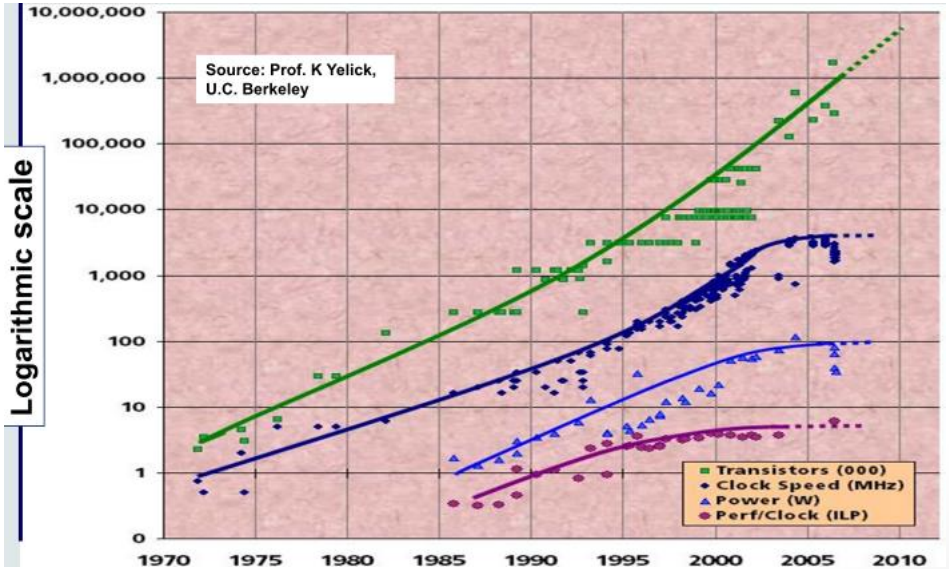
Course Information (Part 2)

Instructor:	Dr. Ahmad El-Banna http://bu.edu.eg/staff/ahmad.elbanna Office: Room #306 Email: ahmad.elbanna@feng.bu.edu.eg
Lectures:	Saturday:14:00-16:30 Prerequisite: ECE505 & Digital Electronics course
Office Hours:	Sunday(10:30~11:30),Tuesday(14:00~16:30)&Wednesday (14:00~16:30)
T.A.:	NA
Texts/Notes:	• Lectures slides, available by each lecture, and found online at http://bu.edu.eg/staff/ahmad.elbanna-courses • **The VHDL Cookbook**, *Peter J. Ashenden, 1st edition, 1990.* • **Computer Aided Design of Electronics** *course lecture notes,* Embedded Systems Laboratory, IDA, Linköping University, *2014* • **Synthesis and Optimization of Digital Systems**.*G. de Micheli.*

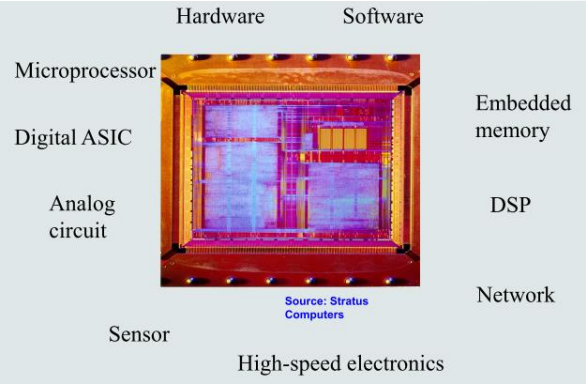
TREND IN MICROELECTRONICS

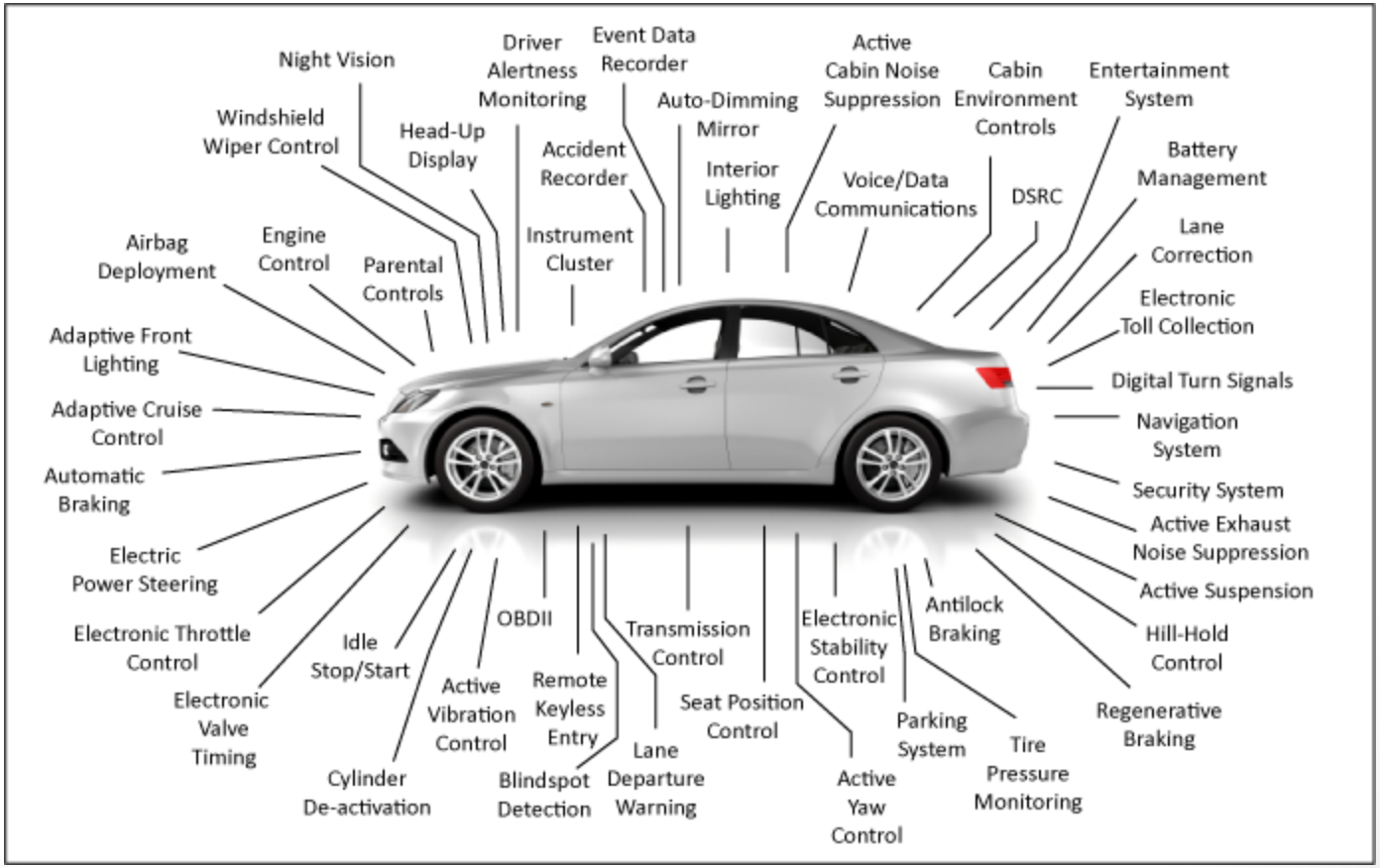
Moore's Law


# of trans.
1000 M
750 M
50 M
25 M
Number of transistors per chip would double every 1.5 years.
Similar improvement in:
Clock Frequency (every 2 years)
Performance
Memory capacity
year
75
80
85
90
95
00
05
10


Source: Prof. K Yelick, U.C. Berkeley
Logarithmic scale
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
0
1970
1975
1980
1985
1990
1995
2000
2005
2010
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)

System on Chip & System of Systems





THE DESIGN CHALLENGES

Many Design Tasks

- System specification (functionality and requirements)
- Hardware/software trade-offs
- Architecture selection and exploration
- Synthesis and optimization
- Implementation
- Testing and design for testability
- Analysis and simulation
- Verification and validation
- Design management: storage of design data,
- cooperation between tools, design flow, etc.

Design Objectives

- Unit cost: the cost of manufacturing each copy of the system, excluding NRE cost.
- NRE cost (Non-Recurring Engineering cost): The one-time cost of designing the system.
- Size: the physical space required by the system.
- Performance: the execution time or throughput .
- Power: the amount of power consumed by the system.
- Testability: the easiness of testing the system to make sure that it works correctly.
- Flexibility: the ability to change the functionality of the system
- without incurring heavy NRE cost.
- Correctness, safety, etc.

The Main Challenges

- System complexity
- Increasing functionality and diversity
- Increasing performance
- Stringent design requirements
- Low cost and low power
- Dependability: reliability, safety and security
- Testability and flexibility
- Technology challenges for cost-efficient implementation
- Deep submicron effects (e.g., cross talk and soft errors)
- Issues related to process variation

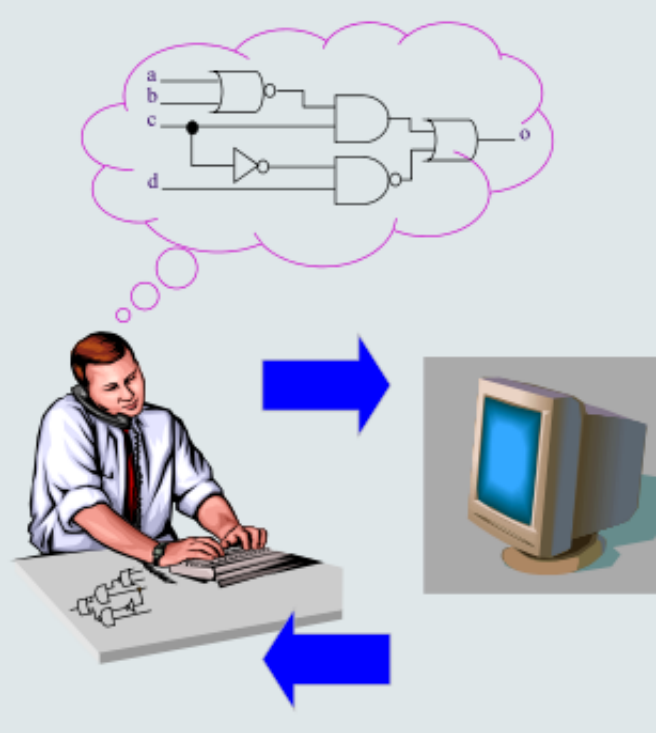
Possible Solutions:

- Powerful design methodology and CAD tools.
- Advanced architecture (modularity).
- Extensive design reuse.

DIFFERENT DESIGN PARADIGMS

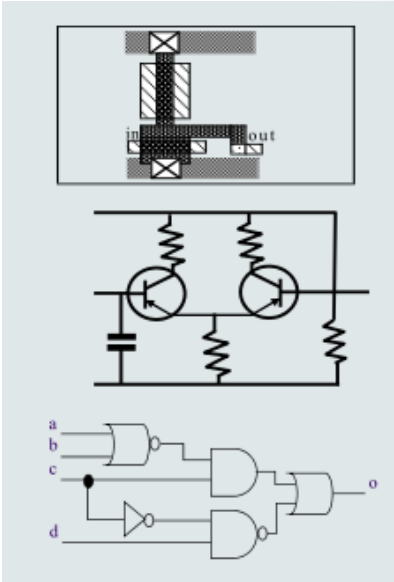
Capture and Simulate

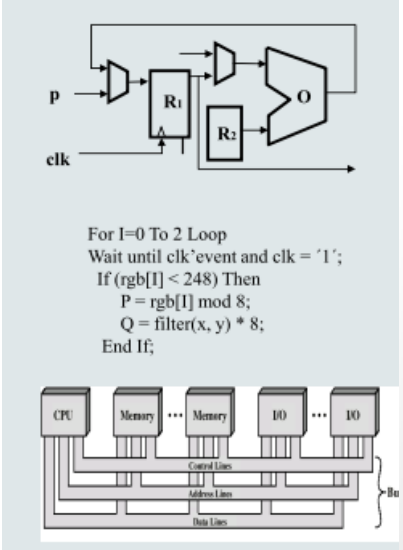
- The detailed design is captured in a model.
- The model is simulated.
- The results are used to guide the improvement of the design.
- All design decisions are made by the designers.



Abstraction Hierarchy

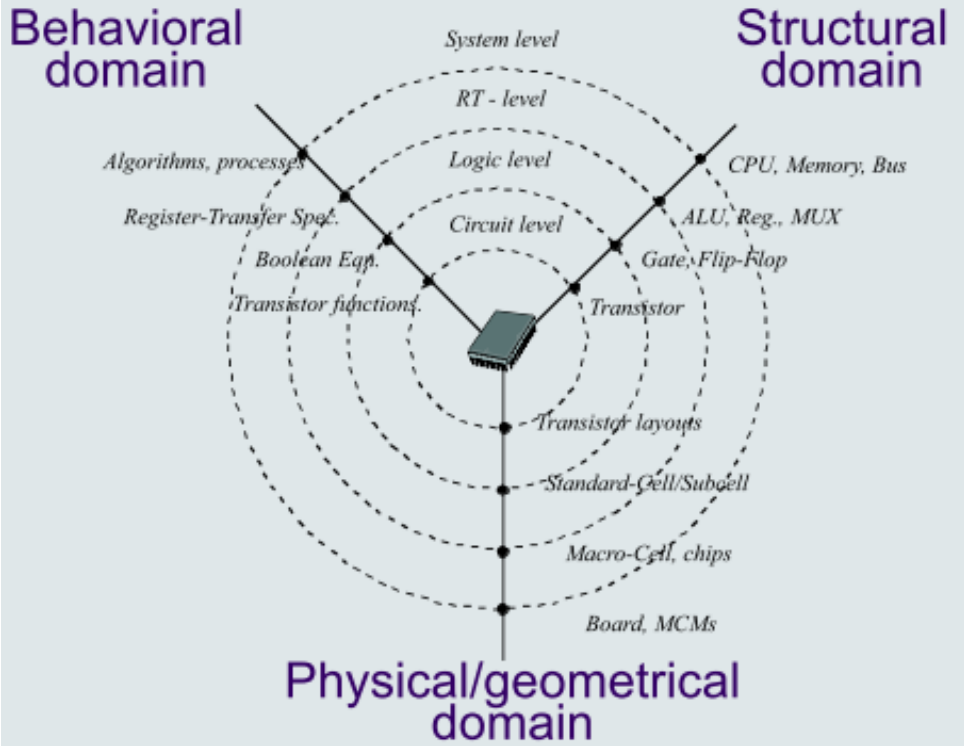
- Layout/silicon level : The physical layout of the integrated circuits is described.
- Circuit level : The detailed circuits of transistors, resistors, and capacitors are described.
- Logic (gate) level : The design is given as gates and their interconnections.
- Register-transfer level (RTL) : Operations are described as transfers of values between registers.
- Algorithmic level : A system is described as a set of usually concurrent algorithms.
- System level : A system is described as a set of processors and communication channels.





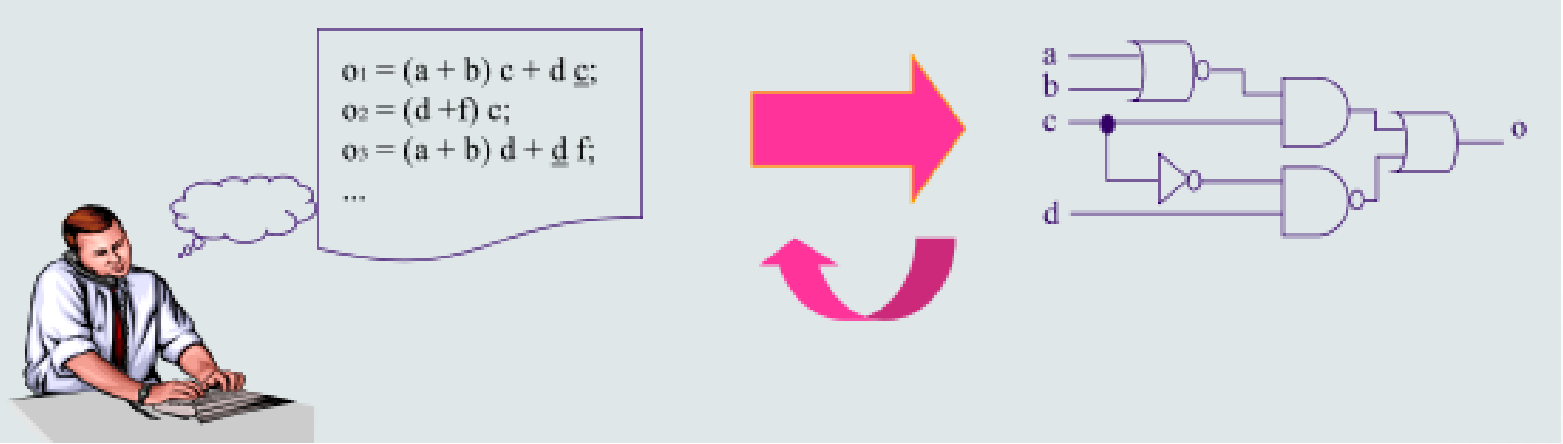
Gajski's Y-Chart

- Behavioral domain — A component is described by defining its input/output functional relationship.
- Structural domain — A component is described in terms on an interconnection of more primitive components.
- Physical/geometrical domain — A component is described in terms of its physical placement and characteristics (e.g., shape).



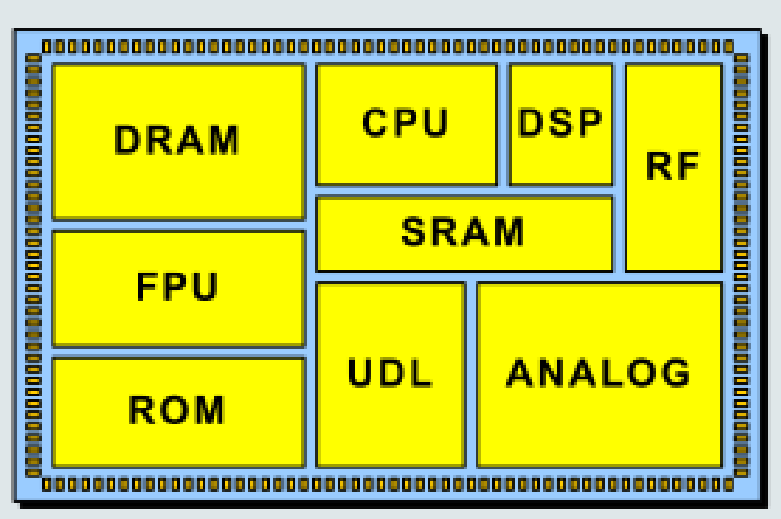
Describe and Synthesize Paradigm

- Description of a design in terms of behavioral specification.
- Refinement of the design towards an implementation by adding structural details.
- Evaluation of the design in terms of a cost function and the design is optimized w.r.t. the cost function.



Core-based Design

- Utilization of pre-designed and pre-verified cores:
  - Reuse of large IP blocks, such as CPU, DSP, memory modules, communication infrastructure, and analog blocks.
- Divide-and-conquer design methodology.
- Flexibility based on different core description levels:
  - Soft: RT level (synthesizable VHDL/Verilog).
  - Firm: Gate-level netlist.
  - Hard: Layout.
- Legal issues:
  - IP right protection.
  - Liability in case of failures.

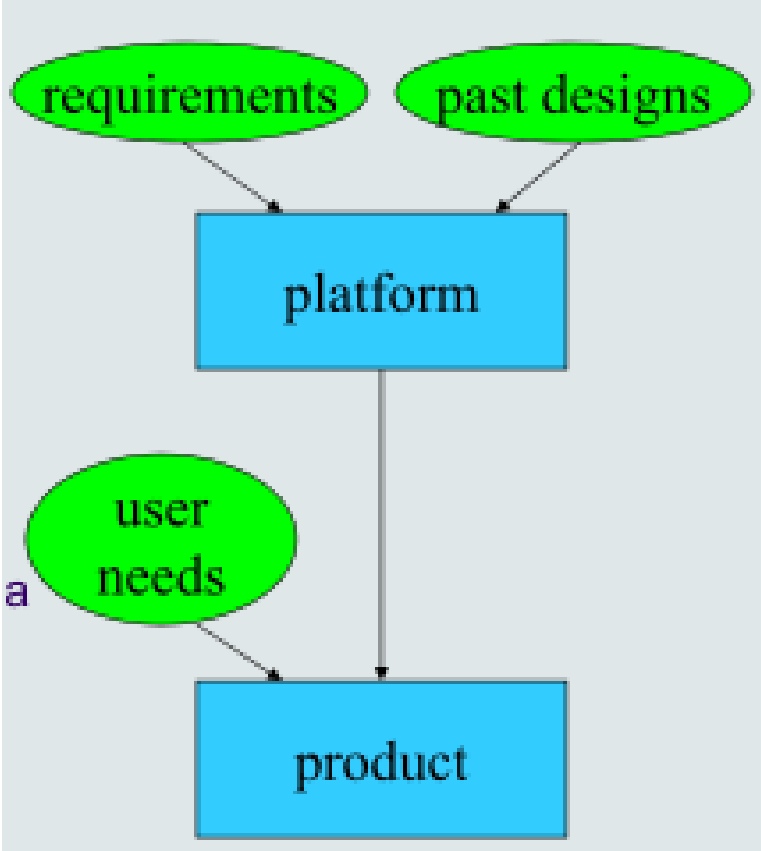


Platform-based Design

- A platform is a partial design:
  - for a particular application area;
  - includes embedded processor(s);
  - may include embedded software;
  - customizable to specific requirements.
- A platform captures the good solutions to the important design challenges in a given application area.
- A method for design re-use at all abstraction levels based on assembling and configuring platform components in a rapid and reliable fashion.
  - It reuses architectures.

Platform-based Design Steps

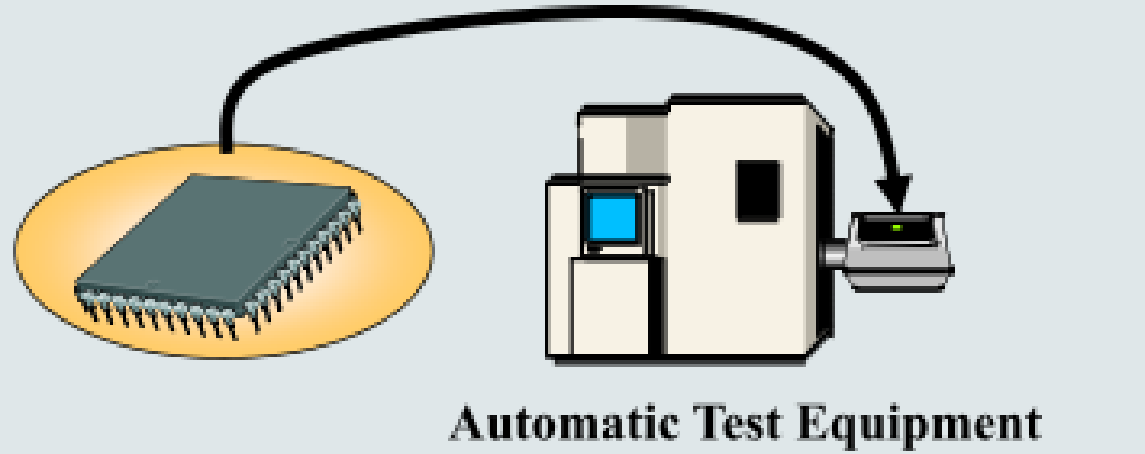
- Design the platform.
  - A highly configurable system architecture.
  - Optimize for performance, power, etc.
  - Useful for a set of applications.
  - Tools to explore the different configurations.
- Use the platform.
  - Modify hardware components for a particular customer's needs.
  - Optimize the software.
  - HW/SW integration and test.



THE TEST PROBLEMS

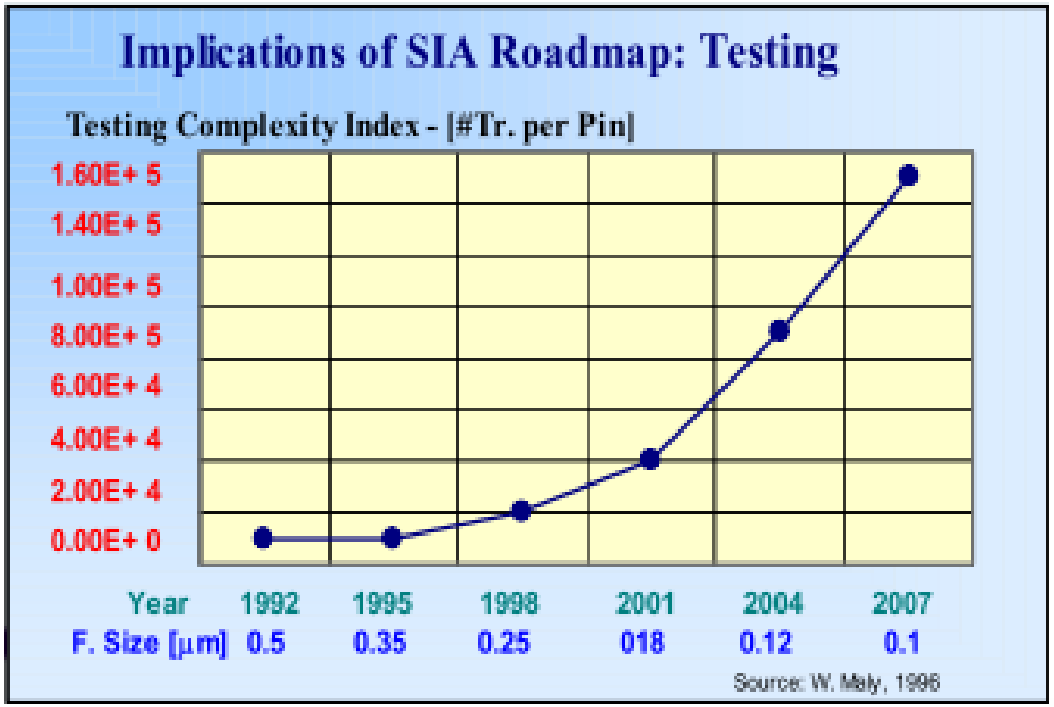
Testing and its Current Practice

- Testing aims at the detection of physical faults (production errors/defects and physical failures).
- Different from the design task, testing is performed on each individual chip, after it is manufactured (volume sensitive).
- The common approach to perform testing is to utilize an Automatic Test Equipment (ATE).



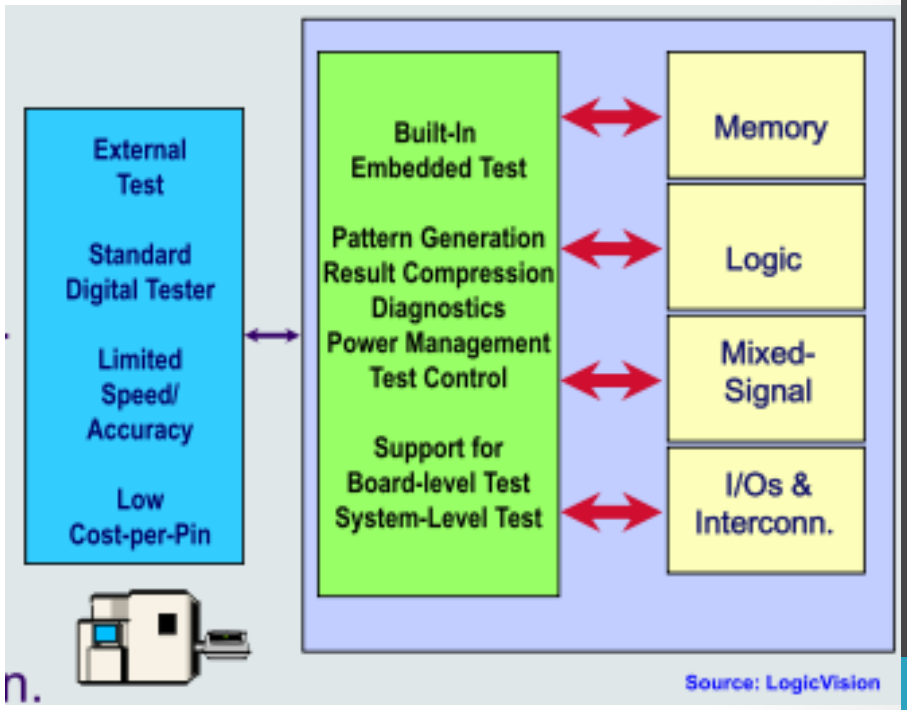
High Test Complexity

- # of transistors increases exponentially.
- # of access port remains stable.
- Implication:
  - Test Complexity Index (# of transistors per pin) increases rapidly.



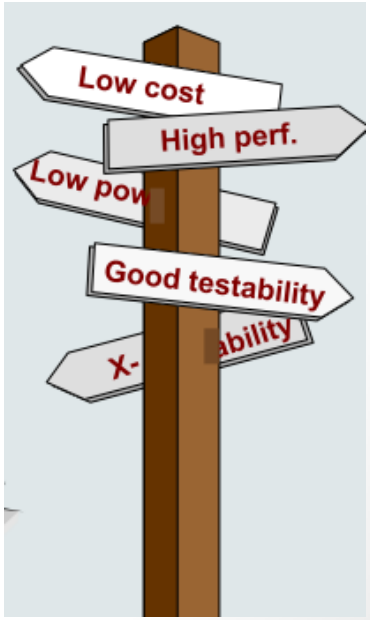
Built-In Self Test (BIST)

- Solution: Dedicated built-in hardware for implementing test functions.
  - No need for expensive
  - ATE.
  - At-speed testing.
  - Concurrent test possible.
  - Support O&M.
  - Support field test and diagnosis
- Design for the best BIST mechanism = optimization.
- Testing => Design



Challenges Still Remain

- System specification with very high-level languages.
- Modeling techniques for heterogeneous system.
- Testing issue to be considered during the design process.
- Design verifications -> get the whole system right the first time!
- Very efficient power saving techniques.
- Design techniques to address process variation.
- Temperature aware design approaches.
- Powerful optimization algorithms.
- Parallel computers for design algorithms.



- For more details, refer to:
  - **Computer Aided Design of Electronics** *course lecture notes*.
  - **The VHDL Cookbook**, *Peter J. Ashenden, 1st edition, 1990.*
- The lecture is available online at:
  - *http://bu.edu.eg/staff/ahmad.elbanna-courses*
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg